

Comparative analysis of memristor devices as neuron

R Manu¹ and Mohammed Riyaz Ahmed²

¹School of ECE, REVA University ²School of Multidisciplinary Studies, REVA University

Abstract

Memristor, a two-terminal device whose unique ability to control its resistance by varying its input, is a promising technological device for intelligent systems. In humans, pattern recognition is associated with memory which helps in decision making for the behavioral and cognitive aspects. The storage of memory is crucial in decision making, and the adaptation between remembering and forgetting memory in time plays a pivotal role for pattern decision; this memory consolidation method is an extreme design challenge in the neuron, the detailed changes in the ion exchange and its timings is what responsible for memory consolidation. A memristor is recognized as a device able to mimic and function like a synapse. Recent advances in memristor have shown the working of a memristor as the different levels of memory, i.e. Long-term memory (LTM) and Short-term memory (STM), memristor devices perform memory potentiation and depression characteristics in them. However, to perform as a real neuron, a network of multiple memristors with careful design has to be followed. In this paper, the detailed mechanism of neuron morphology is explained to show how the many mechanisms inside the biological neuron become responsible for memory consolidation and compare how a memristor can function the neuron rules like plasticity and spike-threshold.

Keywords: Frequency-timing, LTP-LTD, Memory, Memristor

Introduction

In nature, the human brain is considered the most complex structure or system, yet scientists have challenged to create it artificially. Understanding the brain has not been an easy task for neuroscientists; it poses many challenges in understanding its design and morphology. The brain alone consists of more than 100 billion neurons with an average of 10000 synaptic connections, making it more than 100 trillion synapses. Though the communication in the biological neurons remains unknown, it can be understood by studying various levels of neural organizations like senses, neural networks, single cells, synapses, membranes, channels, ions, and genes [1]. Neurons are the building blocks for learning, memory and decision making. A new emerging interdisciplinary field called neuromorphic engineering is involved in understanding the betterment of the human brain in designing the hardware models of neuronal and sensory systems by taking inspiration from biology, physics, mathematics, neuroscience, psychology, cognition, nanotechnology, computer science, robotics and more. Neuromorphic engineering was first introduced as a branch of analogue circuit engineering [2]. It involves developing hardware models and systems to mimic the human brain to achieve efficiency in energy, high parallelism, retention capacity, and tasks involved in cognition like association, recognition, adaptation, and learning [3]. A promising neuromorphic hardware device called a memristor works as an analog-digital system that performs functions similar to neuron characteristics in the brain [4]. The brain-inspired Artificial Neural Networks (ANN's), machine learning has shown a significant promise in building human intelligence in the software domain. However, the hardware platform in scaling is lagging, and one of the reasons is Moore's law limitation. The memristor here could be the next alternative device to the transistor [10]. In section 2 of this paper, a brief overview of the memristor device's working and characteristics is briefed. Then, in section 3, an overview of existing memory literature regarding its neuron physiology is discussed. Finally, in section 4, we have reviewed existing literature memristor device papers which show plasticity nature.

Memristor

The fundamental circuit variables that we know of are current, voltage, electric charge and magnetic flux. However, an interdepending relationship exists between these variables to form passive devices like a resistor, capacitor, and inductor, and there is a missing link between charge and flux. In 1971 a scientist named Leon O Chua modelled and provided a functional relationship between flux and charge. He prototyped the circuit emulator on a breadboard and named it as memristor [5]. Memristor is a twoterminal non-linear passive device with variable resistance characteristics. It is either a voltagecontrolled or current-controlled device whose resistance is determined by the time history of the voltage across it [6]. In a resistor, the flow of current resistance remains equal when in forward and backward directions. However, when the flow of current is in the opposite directions, the current resistance for both directions can be of different values [7][8][9]. In a memristor, when the input power is turned off, the resistance in it freezes, and when the device is activated again, the device resistance would still be the same as the previous one [7][8][9]. Imagine a water pipe; the amount of current flowing through the pipe is large. If the mouth diameter of the pipe is large, that means even the resistance is negligible. On the other hand, the amount of current flowing through the pipe is small when the pipe's mouth diameter is small, which means the resistance is considerable. In a typical resistor, the pipe diameter remains constant. The diameter does not change by the flow of current in any direction, but in memristor, the shrinking and expansion of the pipe's mouth (diameter) happens with the direction of flow of current. However, when there is no current flow, the pipe can remember its previous diameter, and when the current starts flowing again, the change in the pipe diameter starts from the time the current flow was turned off (current freezes). Now, this is how it can "remember" the amount of charge that has gone through it [7][8][9]. The property of retaining the previous information even when there is no power, the "remembering" property, makes this device unique. Although Leon Chua had realized the memristor model on a breadboard, its complete story and potential were only known to the world in 2008 when a research team in HP labs led by Stanley Williams fabricated, modelled and gave its mathematical details in the device's nanometer scale. Then, based on keeping Moore's law going, they began to model two-terminal molecular devices in nanoscale. While they were trying to build, they came up with a device model which consisted of a monolayer of TiO2 between two crossed nanowires, and those nanowires were Pt electrodes. When they applied positive voltage to one side of the electrode, they found out that the TiO2 layer got divided into two, and the layer close to the +ve electrode lacked few oxygen atoms. Those ions formed a bridge and connected towards the opposite Pt electrode (working as a synapse), conduction happened between the two layers, and low resistivity was seen. Nevertheless, to their surprise, they had thought it would be ion formation in the opposite direction when -ve voltage is applied, but it did not. When -ve voltage was applied in Pt electrode, the oxygen atoms got attracted towards itself, and no bridged formation single-layered here existed no conduction between them, so because of this high resistance was seen. The top layer acts as a conductor, and the bottom acts as an insulator [7][10]. Since its discovery, much interest has progressed, and other than just TiO2 based model, many other models have been found [11].

Memristor Characteristics

From Strukov et al.'s study of crossbar nanolayer architecture, multiple layers of memristor can be stacked on one another. Transistors are single-layered, but crossbar architecture is an approach to place a multilayer number of crossbar memories of memristor layers, layer by layer, one above another on a single chip [12]. Crossbar nanostructures, as in Fig.1 [13], has got high scalability, flexibility, and high density [14] which allows a large number of computations to be performed [15]; multiple wide layers help in handling deep layered neural networks for complex tasks and models.



Figure 1. A memristor active layer switch is present across the horizontal wires (electrodes)

The data swap between the von Neumann architecture computers separately placed memory and processing generates high heat and energy [16]. If we follow this type of digital approach, running humanlevel intelligent applications on a device would require power more than 10MW of energy [17]. The size of a transistor is inversely proportional to switching speed [18], memristor has a high switching speed character (spike-based technique) [19], low heat generation, low power consumption [20], and due to less input voltage requirement, it dissipates lesser energy [21]. Due to high switching ability, the storage retention can be up to a lifetime [19]. In 2010, HP labs fabricated a 3nm memristor switch with a speed of approximately one nanosecond that could have a storage capacity of 128 terabytes per centimeter square [22]. Memristor runs on an analog continuum [23] device with fuzzy logic property (any real value that ranges between 0 and 1), which is an essential property for many AI systems [24]. Fabrication of these devices are possible in Nano-imprint-lithography techniques, and these methods are expensive methodology to manufacture, which involves several fabrication steps [25]. Memristor could impact the emerging fields in electronic industries like 5G and IOT, which are in huge demand for data storage methods [26].

Memory

Communication is the fundamental aspect of a neuron, and it is through the modulation of signals in these neurons, learning and memory are interpreted and modulated. Learning and memory are interdependent [27]. The change in the learning alters the memory and vice versa. In the brain, for any operation of any function, the memory plays a vital role; the data for human memory is received and processed by the changing environment through sense organs [28], this received information is subjected to learning. The learning process is determined and affected by environmental, cognitive, and behavioral factors like attention, recognition, remembering, imagination, thinking, background noise, concentration. These factors become responsible for affecting the input frequency timing and the time intervals of received signals. Based on the rate of input frequency timing and time intervals of the signal, the strength of the neuron is determined, and this input which affects the memory, is further classified into short-term memory (STM) and long-term memory (LTM).

Neuron Morphology

The resting potential of the neuron membrane is approximate -70mV, and the change in its membrane potential is caused by the type of ions that enter through the channels [29]. Two types of signals enter the neuron - excitatory signals and inhibitory signals. The excitatory signal causes the entry of Na+ ions through the NMDA channel, which excites the neuron membrane. In contrast, the inhibitory signals cause the entry of Cl- ions through the GABA channel, which inhibits the neuron membrane. This change in the polarity of ionic polarization causes the shift of electric charge in the membrane, and when the combined membrane

potential reaches -55mV, the depolarization begins as in Fig.2(a). Furthermore, it causes the neuron to generate an all or none spike at the axon hillock called an action potential, which is nothing but an impulse of charged ions along the axon.

Figure 2 At the threshold point of -55mV the neuron depolarization activates (b.) lons transmitting and receiving mechanism in synapse



(b.)

The action potential or the train of action potentials travel along the axon in the form of exchange of ions and activates the calcium channels present at the end of the pre-synaptic neuron terminal; the activation of calcium channels causes an influx of Ca2+ ions inside the membrane of pre-neuron, these Ca2+ ions trigger the synaptic neurotransmitter vesicles [30] and releases the transmitters like Na+ and Cl- into the synaptic cleft.

The neurotransmitters released into the synaptic cleft trigger the receptor channels like NMDA and GABA present on the membrane of post-neuron to open it, and depending on the polarity of ions that enter through those channels, the signal transmission of post-neuron will be excitatory synaptic transmission or inhibitory synaptic transmission.

Signal Input Frequency and Timing

The factors which make a memory "the memory" is the rate of frequency and the timing of the input signals. A neuron gets converted from short term memory (STM) to long term memory (LTM) based on the frequency input the neuron receives, also known as memory consolidation. Synaptic plasticity is the foundation of learning and memory. The synapse's efficacy or strengthening and weakening is modified based on its activity over time [31]. The weights or efficacy of synapse is the communication strength between the adjacent neurons, and this depends mainly on the volume and type of neurotransmitters released during the exocytosis process in the presynaptic neuron. The number of receptors activated in the postsynaptic neuron by those neurotransmitters [32] Fig.2(b). All excitatory synapses express different synaptic plasticity forms [31]. Depending on the shape and size of external pulses, the plasticity is of two types, short-term plasticity (STP) and long-term plasticity (LTP) [33]. Spike frequency adaptation [SFA] is an

activation process that lowers its spike frequency over time for sustained excitatory input. Adaptation in a neuron is a vital phenomenon responsible for memory consolidation, this process takes place for an adapting neuron when a powerful input current or voltage step exists, and the neuron fires continuously repeated spikes. However, each subsequent spike will be longer in period than the previous spike [35] (in biological neurons, this is also known as spike-broadening [36]). In neurons at the region of the presynaptic axon terminal, the action potential duration affects the calcium channel resulting in changing the probability of Ca2+ ions influx inside the cytoplasm, which in turn affects the probability of the release of neurotransmitters into the cleft during the exocytosis process [31] [37].

Based on adaptation, short term spikes enhancement exists in numerous phases in order of time and rate of frequency. Approximate values of short-term enhancements can be referred from [33][36][40].

Due to the change in environment, the neuron exhibits spike adaptation, and through this adaptation, the learning and memory exhibits; this adaptive learning is responsible for a mechanism called Hebbian synaptic plasticity. This mechanism has two approaches of learning (1) Spike-rate- dependent plasticity (2) Spike-time-dependent plasticity [39]. The spike-dependent plasticity generates two forms of memory states, long term potentiation (LTP) and long-term depression (LTD) [40]. In the neurons, when a presynaptic spike occurs, approx. 10 to 30ms before the postsynaptic spikes, then it is long-term potentiation (LTP), and if the postsynaptic spike occurs approx. 20 to 100ms before the presynaptic spike is long-term depression (LTD) [41]. During LTP, the synapse strength between the two neurons increases and when the mismatch occurs during LTD, the synapse strength decreases. This strengthening and weakening of synapses strictly depend upon the rate of time and the level of signal frequency. For example, when high-frequency tetanus like 100Hz is stimulated for 15min only, the LTD is induced [42]. For memory and learning, LTP is a necessary mechanism for remembering, as much as the LTD mechanism is for forgetting [43].

Memristor as Neuron

Memristor Ion-Channel Formation

In biological neurons, the signal is generated as analog while its spike generates digitally. Therefore, the dynamics of ion channels play a significant role in plasticity. In the case of implementing plasticity on a hardware domain, much progress has been seen on physical mechanisms and the materials of memristive devices using different ion transportation approaches [44]. A memristor is a time-invariant device whose memristance can be controlled by varying the input voltage or current [45]. Memristor is physically structured as electrode/insulator/electrode, depending on the input polarity and strength. The ions migrate from one electrode to another [46]; this mechanism is similar to synapse in a neuron.

The approach in building memristive switches has been very complex because of the physics of the device like electric field effect, drift velocity of ions [47], mobility of electrons, device thickness, switching time, forming voltages, input voltage or current effect, temperature [48]. The ion transportation mechanism in a memristor is available in many forms of switching technologies like Resistive Random-access memory (ReRAM), Conductive bridge random access memory (CBRAM), Phase change memory (PCM), oxygen displacement memory (OxRAM), Ferroelectric random-access memory (FRAM), and some other approaches. Based on the type of switching and material used, the mechanism proposed in the insulating layers could be charge trap/de trap, conductive filament formation, oxygen vacancy migration, and more. The operation of the switching mechanism happens through a breakdown rupture of the conductive

filament of its insulating layer. In [49] detailed discussion about switching materials and their ion formation mechanisms is given.

Spike Threshold Mechanism

The resting potential of the soma region in the neuron is almost -70mV, the incoming ions vary the membrane potential in the region and if more number of positive ions entered the cytoplasm and when the total electric voltage is now integrated and if the potential of the region is at the threshold point, i.e., 55mV then we see an abrupt depolarization called threshold spike. The threshold switching and memory are considered independent and different, and their connection is rarely discussed [49]. However, such a threshold switching mechanism has been observed in some of the binary switching oxide materials like NbO2 [50][51], TiO2 [52], HfO2 and [53].

In a study by Pickett and Williams at HP Labs [50] for NbO2 material, the switching is thermally driven insulator-to-metal phase transition (IMT), displayed threshold switching character. In this, the device's resistance is dropped instantly at a bias threshold, and the joule heating induces filamentary formation across the device. The model was compatible with transistors in terms of speed and power requirements; the fabricated device showed switching ON in just sub-nanosecond times with total switching energy of approximately 100fJ, the model in SPICE simulation showed character for 10 nm radius devices that it could perform switching in tens of picosecond with energies of just tens of femtoseconds. This IMT model mechanism of the NbO2 device is, in fact, the most widely used temperature-driven transition model for threshold switching [54].

Figure 3. In the circuit the red arrows denote charging loop and discharging loop. Reused with permission from Ref. [55] (©[2018] IEEE)



In [55], the authors have expressed a neuron type modelled circuit structure, using resistors and capacitors with an Ag/SiO2/Au fabricated threshold switching device as in Fig.3. For this circuit, a voltage source input series of voltage pulses of 100 Hz frequencies with a width of 7ms and an amplitude of 2V acts as an input. Here the capacitor acts as the membrane potential region of the neuron, which integrates and accumulates the incoming voltage pulses with a set value as threshold point.

The red arrows in the circuit from Fig.3 show the charging loop (CL) and discharging loop (DL). The memristive device is still in a high resistance state (HRS). Once the incoming voltage reaches the set value memristor device switches from HRS to a low resistance state (LRS), and when the device is in LRS, the discharging of the capacitor begins, and this discharging acts as a neuron spike to form the output voltage.

Plasticity

In biological neurons, plasticity is essential for learning and memory; functions like synaptic weight, pulse width, the amplitude of voltage, number of frequencies, time decay affect the plasticity of neurons [56]. In psychological science, Atkinson and Shiffrin modelled a "multistore model" [57] as in Fig.4, according to which the short-term memory (STM) weight changes are a transient response while the long-term memory (LTM) weight changes are permanent. This model also considers that STP can be transformed to LTP over a prolonged period of repeated stimulation [58].



Figure 4. The psychological model of human memory proposed by Atkinson and Shiffrin [57].

Based on the multistore model, the authors of [52] fabricated a bilayer memristor structure and demonstrated successfully that the device transformed itself from STP to LTP when repeated stimulation was induced. The device exhibited instant switching at a higher voltage. However, at a lower voltage or negative voltage, the conductance was able to be tuned, which worked as an analog switching, the device resistance changed from off-state to on-state when bias voltage of +3.5V was applied (SET process) to the top electrode, and the device resistance changed from on-state to off-state when bias voltage of -3.5V is applied (RESET process) working as a typical memristor [10]. In the device, it was also observed that if the bias voltage was reduced to +1.5V or -1.5V, then the memristor conductance was incomplete, and like this, by varying the bias input, the ion-filament position could be modulated. Even if the bias input were low, the following bias would pick up the conductance from the previous position. The positive bias that gradually increases the conductive filament from the top electrode (TE) to the bottom electrode (BE) is considered potentiation, and vice-versa is considered depression. Here the transition of the device from STM to LTM is explained using the pulse train repetition process and its varying amplitude. The train of input pulses maintain intervals; initially, when a pulse train of +1.2V of 10 times with 50ms interval between them, the device behaved as potentiation. After 40 s, the current decreased to its initial state; this behavior was similar to the STP process, which involves the decay of current over time, and following with similar conditions this time, the pulse numbers gradually increased because of which the increase in current was seen. Based on the number of pulses, a more miniature pulse train causes a slight increase in current that functions as STM and a large pulse train increases the current that functions as LTM.

In a recent paper [59], the authors have analyzed and discussed the characteristic paired-pulse-facilitation (PPF), an enhancement version of STM. The modelled memristor device was fabricated on a glass wafer from ITO/ZTO/ITO materials. Here the STM and LTP concepts are explained by the thickness formation of oxide filaments. The pulse characteristics conditions are defined as LTM or STM. For the experiment, when a train of 20 consecutive pulses with the voltage input high (2.6V) and the pulse interval short (0.5us), these conditions create LTM, and when the voltage input is low (2.0V) and longer pulse interval (300us) conditions create STM. The PPF mechanism works when the intervals of the pair pulses are different. For example, when the interval was increased abruptly from 10us to 0.1s, this decreased in current from 19.04% to 1.6%, the decay of current was set according to several pulses stimulated when the pulse interval was the more extended level of current induced was higher.

Discussion

Solid-state memristor fabrication is relatively challenging because of its nanometer size. Extensive workload towards its fabrication has been reported from various organizations like HP, Intel, Knowm, Rain Neuromorphic, and a programable memristor computer reported by Wei D. Lu [60]. Memristor fabrication based on various printing technologies have also been reported [61].

Technical fields like Robotics, Humanoids, and Artificial Intelligence that exist today work on transistor technology are still questions about their ease and performance. In contrast, the analog memristor device, which contains memory functions responsible for creating cognitive and behavioral mechanisms, can make a difference in the way we think of modelling neurorobotics, movies like "Chappie" and "I, Robot" (Sonny) are an example of how a machine can be a human in terms of its behavioral and cognitive functions.

A neuron acts as a system consisting of different necessary mechanisms that are interdependent to perform rules like SFA, STDP, SRDP, memory adaptation, integration and fire, in a similar fashion. One type of memristor or memristor model or memristor ion transportation mechanism is not enough [62]. Classification of multiple memristor families is required to design the system.

Conclusion

Consciousness, generally known as the soul in the human term, is an integral part of human memory. In this paper, we have presented a brief understanding of the memristor device and compared how the memristor is similar to the working physiology of a neuron. We have explained the morphology of neurons detailly to understand the importance affecting the changes in different levels of memory. We discuss how a single memristor device is not enough for the many memory rules. We have reviewed papers that have used different types of memristor devices for memory rules.

REFERENCES

P. Suffczynski, F. Wendling, J. -. Bellanger and F. H. L. Da Silva, "Some Insights Into Computational Models of (Patho)physiological Brain Activity," in Proceedings of the IEEE, vol. 94, no. 4, pp. 784- 804, April 2006, doi: 10.1109/JPROC.2006.871773.

C. Mead, "Neuromorphic electronic systems," in Proceedings of the IEEE, vol. 78, no. 10, pp. 1629-1636, Oct. 1990, doi: 10.1109/5.58356.

Daniele Ielmini, Stefano Ambrogio, "Emerging neuromorphic devices," in IOP Publishing, vol. 31, no. 9, p. 092001, Dec. 2019, doi: 10.1088/1361-6528/ab554b.

Rose, Garrett S and Shawkat, Mst Shamim Ara and Foshie, Adam Z and Murray, John J and Adnan, Md Musabbir, "A system design perspective on neuromorphic computer processors," in IOP Publishing, Sept. 2021, doi:10.1088/2634-4386/ac24f5., in press.

L. O. Chua, "Memristor—The Missing Circuit Element," IEEE Trans actions on Circuit Theory, Vol. 18, No. 5, 1971, pp. 507-519.

Liu, Weizhen & Jiang, Minghui & Yan, Meng, "Stability analysis of memristor-based time-delay fractional-order neural networks,". Neurocomputing. vol. 323, pp. 117-127, Jan. 2019, doi: 10.1016/j.neucom.2018.09.073.

Vahid Keshmiri, "A Study of the Memristor Models and Applications," 2014.

Raj B., Vaidyanathan S, "Analysis of Dynamic Linear Memristor Device Models,". Springer, In: Vaidyanathan S., Volos C. (eds) Advances in Memristors, Memristive Devices and Systems Studies in Computational Intelligence, vol. 701, pp. 449-476, Feb. 2017

R. S. Williams, "How We Found The Missing Memristor," in IEEE Spectrum, vol. 45, no. 12, pp. 28-35, Dec. 2008, doi: 10.1109/MSPEC.2008.4687366.

Dmitri B. Strukov, Gregory S. Snider, Duncan R. Stewart, R. Stanley Williams, "The missing memristor found,". Nature, vol 453, pp. 80-83, May. 2008, doi: 10.1038/nature06932

Yakopcic C, Taha T.M, Subramanyam G, Pino R.E, "Memristor SPICE Modeling", In: Kozma R., Pino R., Pazienza G. (eds) Advances in Neuromorphic Memristor Science and Applications. Springer Series in Cognitive and Neural Systems, vol 4. Springer, Dordrecht, 2012.

Dmitri B. Strukov, R. Stanley Williams, "Four-dimensional address topology for circuits with stacked multilayer crossbar arrays," in Proceedings of the National Academy of Sciences, vol. 106, pp. 20155 - 20158, 2009.

Sung Hyun Jo, Kuk-Hwan Kim, Wei Lu, "High-density crossbar arrays based on a Si memristive system", Nano Lett., vol. 9, pp. 870- 874, 2009.

Shuang Pi, Can Li, Hao Jiang, Weiwei Xia, Huolin Xin, J. Joshua Yang, Qiangfei Xia, "Memristor crossbar arrays with 6-nm half-pitch and 2- nm critical dimension", Nature Nanotech, vol. 14, pp. 35-39, 2019, doi: 10.1038/s41565-018-0302-0.

G. Papandroulidakis, I. Vourkas, A. Abusleme, G. C. Sirakoulis and A. Rubio, "Crossbar-Based Memristive Logic-in-Memory Architecture," in IEEE Transactions on Nanotechnology, vol. 16, no. 3, pp. 491-501, May 2017, doi: 10.1109/TNANO.2017.2691713.

R. Nair, "Evolution of Memory Architecture," in Proceedings of the IEEE, vol. 103, no. 8, pp. 1331-1345, Aug. 2015, doi: 10.1109/JPROC.2015.2435018.

R Douglas, M Mahowald, C Mead, "Neuromorphic Analogue VLSI," in Annual Review of Neuroscience, Vol. 18, pp. 255-281, March. 1995, doi: 10.1146/annurev.ne.18.030195.001351

A. Sleiman, P.W. Sayers, D.A. Zeze, M.F. Mabrook, "Two-terminal organic nonvolatile memory (ONVM) devices," in Handbook of Flexible Organic Electronics, Stergios Logothetidis, Ed., Oxford, Woodhead Publishing, pp. 413- 428, 2015, doi: 10.1016/B978-1-78242-035-4.00017-8

Dmitri B. Strukov, R. S. Williams, "Exponential ionic drift: fast switching and low volatility of thin-film memristors," in Springer, vol. 94, pp. 515-519, 2009, doi: 10.1007/s00339-008-4975-3.

K L Wang, J G Alzate, P Khalili Amiri, "Low-power non-volatile spintronic memory: STT-RAM and beyond," in IOP Publishing, vol. 46, no. 7, p. 074003, Feb. 2013, doi: 10.1088/0022-3727/46/7/074003

S. Pal, V. Gupta, W.H. Ki, A. Islam, "Design and development of memristor-based RRAM," in IET Circuits Devices Syst., vol. 13, pp. 548-557, May. 2019, doi: 10.1049/iet-cds.2018.5388

D. B. Strukov et al., "Hybrid CMOS/memristor circuits," 2010 IEEE International Symposium on Circuits and Systems (ISCAS), 2010, pp. 1967-1970, doi: 10.1109/ISCAS.2010.5537020.

L. Chua, "Five non-volatile memristor enigmas solved,". Springer. Appl. Phys. A, vol. 124, July. 2018, doi: 10.1007/s00339-018-1971-0

D. Bhattacharjee, W. Kim, A. Chattopadhyay, R. Waser, V. Rana, "Multi-valued and Fuzzy Logic Realization using TaOx Memristive Devices,". Nature. Scientific Reports, vol. 8, Jan. 2018, doi: 10.1038/s41598-017-18329-3

J. J. Yang et al., "Memristive switching mechanism for metal/oxide/metal nanodevices," Nature Nanotechnology, vol. 3, no. 7, pp. 429–433, 2008

5G, IoT, and the data explosion — a storage problem?, Aug. 2018. [Online]. Available:https://techhq.com/2018/08/5g-iot-and-the-data-explosion-an-enterprise-storage-problem/

J. C. Spender, "Organizational knowledge, learning and memory: three concepts in search of a theory," in Journal of Organizational Change Management, vol. 9, pp. 63-78, 1996, doi: 10.1108/09534819610156813.

Guy Rachmuth, Harel Z. Shouval, Mark F. Bear, and Chi-Sang Poon, "A biophysically-based neuromorphic model of spike rate- and timing dependent plasticity," in Proceedings of the National Academy of Sciences, Dec. 2011, doi: 10.1073/pnas.1106161108.

Larry F. Abbott, "Single Neuron Dynamics: an Introduction,". in Neural Modeling and Neural Networks, F. Ventriglia, Ed., Amsterdam: Pergamon Studies in Neuroscience, pp. 57-78, 1994, doi: 10.1016/B978-0- 08-042277-0.50009-5

Thomas C Sudhof, "Calcium control of neurotransmitter release," Cold " Spring Harb Perspect Biol. vol. 4, Jan. 2012, doi: 10.1101/cshperspect a011353.

Ami Citri, Robert C Malenka, "Synaptic Plasticity: Multiple Forms, Functions, and Mechanisms," in Proceedings of Nature. Neuropsychopharmacology, vol. 33, pp. 18-41, Aug. 2007, doi: 10.1038/sj.npp.1301559.

Justin Lines, Ana Covelo, Ricardo Gomez, Lan Liu, Alfonso Araque, "Synapse-Specific Regulation Revealed at Single Synapses Is Concealed When Recording Multiple Synapses," in Proceedings of Frontiers in Cellular Neuroscience, vol. 11, p. 367, 2017, doi: 10.3389/fncel.2017.00367.

Takeo Ohno. et al., "Short-term plasticity and long-term potentiation mimicked in single inorganic synapses," Nature Mater, vol. 10, pp. 591- 595, 2011, doi :10.1038/nmat3054.

Zucker, Robert S, Wade G Regehr, "Short-term synaptic plasticity." Annual review of physiology, vol. 64, pp. 355-405, 2002, doi: 10.1146/annurev.physiol.64.092501.114547.

J. V. Arthur and K. A. Boahen, "Silicon-Neuron Design: A Dynamical Systems Approach," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 5, pp. 1034-1043, May 2011, doi: 10.1109/TCSI.2010.2089556.

M Ma, J Koester, "The role of K+ currents in frequency-dependent spike broadening in Aplysia R20 neurons: a dynamic-clamp analysis," The Journal of neuroscience: the official journal of the Society for Neuroscience, vol: 16, 1996, doi: 10.1523/JNEUROSCI.16-13-04089.

Ma M, Koester J, "Consequences and mechanisms of spike broadening of R20 cells in Aplysia californica," The Journal of Neuroscience : the Official Journal of the Society for Neuroscience, vol. 15, no. 10, pp. 6720-6734, Oct. 1995, doi: 10.1523/jneurosci.15-10-06720.1995.

Hardy Hagena, Denise Manahan-Vaughan, "Frequency Facilitation at Mossy Fiber–CA3 Synapses of Freely Behaving Rats Contributes to the Induction of Persistent LTD via an Adenosine-A1 Receptor-Regulated Mechanism," Cerebral Cortex, Vol. 20, pp. 1121–1130, May. 2010.

S. Vidya and M. R. Ahmed, "Advent of memristor based synapses on neuromorphic engineering," 2017 International conference on Microelectronic Devices, Circuits and Systems (ICMDCS), 2017, pp. 1-6, doi: 10.1109/ICMDCS.2017.8211706.

H Markram, J Lubke, M Frotscher, B Sakmann, "Regulation of synaptic " efficacy by coincidence of postsynaptic APs and EPSPs." Science, vol. 275, pp. 213-215, doi: 10.1126/science.275.5297.213.

D.E. Shulz, D.E. Feldman, "Spike Timing-Dependent Plasticity," in Neural Circuit Development and Function in the Brain, John L.R. Rubenstein and Pasko Rakic, Ed., Oxford: Academic Press, 2013, pp. 155-181

Shouval Harel, Wang Samuel, Wittenberg Gayle, "Spike Timing Depen dent Plasticity: A Consequence of More Fundamental Learning Rules," Frontiers in Computational Neuroscience, vol. 4, p. 19, 2010, doi: 10.3389/fncom.2010.00019.

Chater Thomas E., Goda Yukiko, "The role of AMPA receptors in postsynaptic mechanisms of synaptic plasticity," Frontiers in Cellular Neuroscience, vol. 8, p. 401, 2014, doi: 10.3389/fncel.2014.00401.

Teng Zhang et al., "Memristive Devices and Networks for Brain-Inspired Computing," physica status solidi (RRL) – Rapid Research Letters, vol. 13, no. 8, p. 1900029, 2019, doi: 10.1002/pssr.201900029.

M. P. Sah, H. Kim and L. O. Chua, "Brains Are Made of Memristors," in IEEE Circuits and Systems Magazine, vol. 14, no. 1, pp. 12-36, Firstquarter 2014, doi: 10.1109/MCAS.2013.2296414.

Xiaoning Zhao, Zhongqiang Wang, Haiyang Xu, Yichun Liu, "Two terminal optoelectronic memory device," in Book title: Photo Electroactive Nonvolatile Memories for Data Storage and Neuromorphic Computing. Series: Woodhead Publishing Series in Electronic and Optical Materials, Su-Ting Han and Ye Zhou, Ed., Woodhead Publishing, pp. 75-105, 2020, doi: 10.1016/B978-0-12-819717-2.00004-7.

G. S. Rose, R. Pino and Q. Wu, "A low-power memristive neuromorphic circuit utilizing a global/local training mechanism," The 2011 International Joint Conference on Neural Networks, 2011, pp. 2080-2086, doi: 10.1109/IJCNN.2011.6033483.

G Dearnaley, A M Stoneham, D V Morgan, "Electrical phenomena in amorphous oxide films," in IOP Publishing, vol. 33, no. 3, pp. 1129- 1191, Sept. 1970, doi: 10.1088/0034-4885/33/3/306

Jae Sung Lee1, Shinbuhm Lee2, Tae Won Noh, "Resistive switching phenomena: A review of statistical physics approaches," in Applied Physics Reviews, vol. 2, 2015, doi: 10.1063/1.4929512.

Matthew D Pickett, R Stanley Williams, "Sub-100 fJ and sub-nanosecond thermally driven threshold switching in niobium oxide crosspoint nanodevices," in IOP Pubishing. Nanotechnology, vol. 23, no. 21, May. 2012, doi: 10.1088/0957-4484/23/21/215202.

E. Cha et al., "Nanoscale (10nm) 3D vertical ReRAM and NbO2 threshold selector with TiN electrode," 2013 IEEE International Electron Devices Meeting, 2013, pp. 10.5.1-10.5.4, doi: 10.1109/IEDM.2013.6724602.

Dongyang Li et al., "Synaptic learning and memory functions in SiO2:Ag/TiO2 based memristor devices," IOP Publishing, vol. 53, no. 17, p. 175102, Feb. 2020, doi: 10.1088/1361-6463/ab70c9.

Kyung Seok Woo et al., "A True Random Number Generator Using Threshold-Switching-Based Memristors in an Efficient Circuit Design," Advanced Electronic Materials, vol. 5, no. 2, p. 1800543, doi: 10.1002/aelm.201800543

Jaehyuk Park et al, "Multi-layered NiOy/NbOx/NiOy fast drift-free threshold switch with high Ion/Ioff ratio for selector application," Scientific Reports, vol 7, 2017, doi: 10.1038/s41598-017-04529-4.

X. Zhang et al., "An Artificial Neuron Based on a Threshold Switching Memristor," in IEEE Electron Device Letters, vol. 39, no. 2, pp. 308-311, Feb. 2018, doi: 10.1109/LED.2017.2782752.

Wen Huang et al., "Memristive Artificial Synapses for Neuromorphic Computing," in Springer. Nano-Micro Letters, vol. 13, no. 85, 2021, doi: 10.1007/s40820-021-00618-2.

Richard M. Shiffrin, Richard C. Atkinson, "Storage and retrieval process in long-term memory," 2005, doi: 10.1037/h0027277.

Guo-qiang Bi, Mu-ming Poo, "Synaptic Modifications in Cultured Hippocampal Neurons: Dependence on Spike Timing, Synaptic Strength, and Postsynaptic Cell Type," in Society for Neuroscience, vol. 18, 1998, doi: 10.1523/JNEUROSCI.18-24-10464.1998.

Ji-Ho Ryu et al., "Bio-inspired synaptic functions from a transparent zinc-tin-oxide-based memristor for neuromorphic engineering," in Applied Surface Science, vol. 544, p. 148796, 2021, doi: 10.1016/j.apsusc.2020.148796.

Fuxi Cai, Wei D. Liu et al., "A fully integrated reprogrammable memristor–CMOS system for efficient multiply– accumulate operations," in Nature Electronics, vol. 2, pp. 290- 299, 2019, doi: 10.1038/s41928- 019-0270-x.

S. Ali, S. Khan, A. Khan and A. Bermak, "Memristor Fabrication Through Printing Technologies: A Review," in IEEE Access, vol. 9, pp. 95970-95985, 2021, doi: 10.1109/ACCESS.2021.3094027.

Mohammad SaeedFeali, "Using volatile/non-volatile memristor for emulating the short-and long-term adaptation behavior of the biological neurons," Neurocomputing, vol. 465, pp. 157-166, 2021, doi: 10.1016/j.neucom.2021.08.132.